REMARKS

This paper is responsive to the Non-Final Office Action dated March 24, 2005. Claims 1-3, 5-23, 25-27 and 30-36 were examined. Claims 1-3, 5-7, 9, 13, 19, 20, 23, 25-27, 35, and 36 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Application Publication US 2004/0008056 A1 to Kursun et al. Claims 21 and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kursun et al. in view of U.S. Patent No. 6,366,132 to Karnik et al. Claims 8, 10-12, and 14-18 are objected to as being dependent upon a rejected base claim. Claims 30-34 are allowed.

Rejections Under 35 U.S.C. § 102

Claims 1-3, 5-7, 9, 13, 19, 20, 23, 25-27, 35, and 36 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Application Publication US 2004/0008056 A1 to Kursun et al. Regarding claim 1, Applicants respectfully maintain that Kursun, alone or in combination with other references of record, fails to teach or suggest that

> the effective strength of a keeper circuit operating on a dynamic node is reduced from a first non-zero strength level to a second non-zero strength level during an interval in which at least one path in an evaluation circuit is sensitive to a keeper device,

as required by claim 1. The Office Action relies on Figure 12 and corresponding portions of the specification of Kursun to supply this teaching. These portions of Kursun teach "a low swing domino logic with a weakly driven keeper circuit technique (LSDWDK)" (paragraph [0078], lines 1-3). "The output voltage swing is between ground and V_{DD}-V_{tn}...The gate voltage of the keeper P2128 swings between $|V_{tp}|$ and V_{DD} (assuming $|V_{tp}| \leq V_{tn}$)" (paragraph [0079], lines 5-9). Keeper transistor P2 of FIG. 12 (labeled 124 by the Office Action) of Kursun is enabled and disabled by the signal on Node 1, i.e., a signal that swings between $|V_{tp}|$ and V_{DD} (assuming $|V_{tp}| \leq V_{tn}$). The signal on the gate of keeper transistor P2 of FIG. 12 of Kursun is $|V_{tp}|$ when Clock is '0' and may be $|V_{tp}|$ or V_{DD} when Clock is '1', depending upon the effects of Pulldown Network 214 (as labeled by the Office Action) on the Dynamic node. Keeper transistor P2 of

FIG. 12 of Kursun is on when Node 1 is $|V_{tp}|$ and off when Node 1 is V_{DD}. When keeper transistor P2 of FIG. 12 of Kursun is off (i.e., when Clock is '1' and Pulldown Network 214 evaluates), the keeper circuit has a strength of zero on the Dynamic node. Thus, Kursun fails to teach or suggest that the effective strength of a keeper circuit operating on a dynamic node is reduced from a first non-zero strength level to a second non-zero strength level during an interval in which at least one path in an evaluation circuit is sensitive to a keeper device, as required by claim 1. For at least this reason, Applicants respectfully maintain that claim 1 distinguishes over Kursun and all references of record. Accordingly, Applicants respectfully request that the rejection of claim 1 and all claims dependent thereon, be withdrawn.

Regarding claim 5, Applicants respectfully maintain that Kursun, alone or in combination with other references of record, fails to teach or suggest that

> a keeper circuit has a first non-zero strength during a first interval and a second non-zero strength during a second interval, the first non-zero strength being substantially greater than the second non-zero strength,

as required by claim 5. The Office Action relies on Figure 12 and corresponding portions of the specification of Kursun to supply this teaching. These portions of Kursun teach "a low swing domino logic with a weakly driven keeper circuit technique (LSDWDK)" (paragraph [0078], lines 1-3). "The output voltage swing is between ground and V_{DD}-V_{tn}...The gate voltage of the keeper P2128 swings between $|V_{tp}|$ and V_{DD} (assuming $|V_{tp}| \leq V_{tn}$)" (paragraph [0079], lines 5-9). Keeper transistor P2 of FIG. 12 (labeled 124 by the Office Action) of Kursun is enabled and disabled by the signal on Node 1, i.e., a signal that swings between $|V_{tp}|$ and V_{DD} (assuming $|V_{tp}| \leq V_{tn}$). The signal on the gate of keeper transistor P2 of FIG. 12 of Kursun is $|V_{tp}|$ when Clock is '0' and may be $|V_{tp}|$ or V_{DD} when Clock is '1', depending upon the effects of Pulldown Network 214 (as labeled by the Office Action) on the Dynamic node. Keeper transistor P2 of FIG. 12 of Kursun is on when Node 1 is $|V_{tp}|$ and off when Node 1 is V_{DD}. When keeper transistor P2 of FIG. 12 of Kursun is off (i.e., when Clock is '1' and Pulldown Network 214 evaluates), the keeper circuit has a strength of zero on the Dynamic node. Thus Kursun fails to

teach or suggest a keeper circuit having a first non-zero strength during a first interval and a second non-zero strength during a second interval, the first non-zero strength being substantially greater than the second non-zero strength, as required by claim 5. For at least this reason, Applicants respectfully maintain that claim 5 distinguishes over Kursun and all references of record. Accordingly, Applicants respectfully request that the rejection of claim 5 and all claims dependent thereon, be withdrawn.

Regarding claim 23, Applicants respectfully maintain that Kursun, alone or in combination with other references of record, fails to teach or suggest

> effectively disabling a first keeper device coupled to the dynamic node during an interval in which at least one path in an evaluation circuit is sensitive to a keeper device and protecting the dynamic node from noise during the interval,

as required by claim 23. The Office Action relies on Figure 12 and corresponding portions of the specification of Kursun to supply this teaching. These portions of Kursun teach "a low swing domino logic with a weakly driven keeper circuit technique (LSDWDK)" (paragraph [0078], lines 1-3). "The output voltage swing is between ground and V_{DD}-V_{tn}...The gate voltage of the keeper P2128 swings between $|V_{tp}|$ and V_{DD} (assuming $|V_{tp}| \leq V_{tn}$)" (paragraph [0079], lines 5-9). Keeper transistor P2 of FIG. 12 (labeled 124 by the Office Action) of Kursun is enabled and disabled by the signal on Node 1, i.e., a signal that swings between $|V_{tp}|$ and V_{DD} (assuming $|V_{tp}| \leq V_{tn}$). The signal on the gate of keeper transistor P2 of FIG. 12 of Kursun is $|V_{tp}|$ when Clock is '0' and may be $|V_{tp}|$ or V_{DD} when Clock is '1', depending upon the effects of Pulldown Network 214 (as labeled by the Office Action) on the Dynamic node. Keeper transistor P2 of FIG. 12 of Kursun is on when Node 1 is $|V_{tp}|$ and off when Node 1 is V_{DD}. When keeper transistor P2 of FIG. 12 of Kursun is off (i.e., when Clock is '1' and Pulldown Network 214 evaluates), the keeper circuit has a strength of zero on the Dynamic node. Thus, Kursun fails to teach or suggest protecting the dynamic node from noise during the interval in which a first keeper device is effectively disabled, as required by claim 23. For at least these reasons, Applicants respectfully maintain that claim 23 distinguishes over Kursun and all references of

record. Accordingly, Applicants respectfully request that the rejection of claim 23 and all claims dependent thereon, be withdrawn.

Regarding claim 27, Applicants respectfully maintain that Kursun, alone or in combination with other references of record, fails to teach or suggest

> means for effectively disabling the first keeper device coupled to the dynamic node during an interval in which at least one path in an evaluation circuit is sensitive to a keeper device and means for protecting the dynamic node from noise during the interval,

as required by claim 27. The Office Action relies on Figure 12 and corresponding portions of the specification of Kursun to supply this teaching. These portions of Kursun teach "a low swing domino logic with a weakly driven keeper circuit technique (LSDWDK)" (paragraph [0078], lines 1-3). "The output voltage swing is between ground and V_{DD}-V_{tn}...The gate voltage of the keeper P2128 swings between $|V_{tp}|$ and V_{DD} (assuming $|V_{tp}| \leq V_{tn}$)" (paragraph [0079], lines 5-9). Keeper transistor P2 of FIG. 12 (labeled 124 by the Office Action) of Kursun is enabled and disabled by the signal on Node 1, i.e., a signal that swings between $|V_{tp}|$ and V_{DD} (assuming $|V_{tp}| \leq V_{tn}$). The signal on the gate of keeper transistor P2 of FIG. 12 of Kursun is $|V_{tp}|$ when Clock is '0' and may be $|V_{tp}|$ or V_{DD} when Clock is '1', depending upon the effects of Pulldown Network 214 (as labeled by the Office Action) on the Dynamic node. Keeper transistor P2 of FIG. 12 of Kursun is on when Node 1 is $|V_{tp}|$ and off when Node 1 is V_{DD}. When keeper transistor P2 of FIG. 12 of Kursun is off (i.e., when Clock is '1' and Pulldown Network 214 evaluates), the keeper circuit has a strength of zero on the Dynamic node. Thus, Kursun fails to teach or suggest means for protecting the dynamic node from noise during the interval in which a first keeper device is effectively disabled, as required by claim 27. For at least these reasons, Applicants respectfully maintain that claim 27 distinguishes over Kursun and all references of record. Accordingly, Applicants respectfully request that the rejection of claim 27 and all claims dependent thereon, be withdrawn.

Rejections Under 35 U.S.C. § 103

Claims 21 and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kursun et al. in view of U.S. Patent No. 6,366,132 to Kamik et al. Applicants respectfully maintain that claims 21 and 22 depend from allowable base claims and are allowable for at least this reason. Accordingly, Applicants respectfully request that the rejection of claims 21 and 22 be withdrawn.

Allowable Subject Matter

Claims 8, 10-12, and 14-18 are objected to as being dependent upon a rejected base claim. Claims 30-34 are allowed.

Applicants appreciate the indication of allowable subject matter in claims 8, 10-12, and 14-18. Applicants respectfully maintain that claims 8, 10-12, and 14-18 depend from allowable base claims and are allowable for at least this reason.

Applicants appreciate the allowance of claims 30-34.

In summary, claims 1-3, 5-23, 25-27 and 30-36 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

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Respectfully submitted,

Nicole Teitler Cave, Reg. No. 54,021
Attorney for Applicant(s)
(512) 338-6315
(512) 338-6301 (fax)